IN THE CLAIMS:

Please cancel claims 3, 4, 9, 10, and amend the claims as follows:

Claim 1 (Currently Amended): A computational unit in an adaptable computing engine, wherein the computational unit includes a clock signal for determining a processor cycle, the computational unit comprising

one or more functional units coupled by a bus, wherein the one or more functional units include functional unit inputs;

at least one pipeline register coupled between the bus and at the input of least one functional unit input;

a control signal for selectively causing the at least one pipeline register to hold a data value from the bus for ~~one or~~ more than one processor ~~cycles~~ cycle at the input of the at least one functional unit, the data value being obtainable at the input at a start of a next processor cycle upon being needed;

a coupling of a pair of pipeline registers such that the pair of registers is responsive to a control signal value; and

control circuitry for setting the pair of pipeline registers into predetermined states based on the control signal value.

Claim 2 (Currently Amended): The computational unit of claim 1, wherein the pipeline register includes circuitry for selectively providing a constant value.

Claims 3-4 (Cancelled)

Claim 5 (Previously Presented): The computational unit of claim 1, wherein the pair of registers includes first and second registers, wherein the predetermined states include one or more of the following for the first and second registers, respectively: load, hold; load, clear; hold, load; clear, load; hold, hold; hold, clear; clear, hold; and clear, clear.

Claim 6 (Currently Amended): The computational unit of claim 1, wherein the control signal value comprises 7 bits to control loading the pairs of pipeline registers as accumulator pair enabling 72 bit operations in the computation unit.

Claim 7 (Currently Amended): A method for providing data in a computational unit in an adaptable computing engine, the method comprising

including pipeline registers at inputs to functional units, wherein the pipeline registers are coupled to a bus for obtaining data from the bus;

including a control signal for selectively causing the pipeline registers to hold a data value from the bus for one or more processor cycles at an input of at least one functional unit in the one or more functional units[[.]], the data value being obtainable at the input at a start of a next processor cycle upon being needed;

coupling a pair of registers such that the pair of pipeline registers is responsive to a control signal value; and

providing control circuitry for setting the pair of pipeline registers into predetermined states based on the control signal value.

Claim 8 (Currently Amended): The method of claim 7, wherein the pipeline register includes circuitry for selectively providing a constant value.

Claims 9-10 (Cancelled)

Claim 11 (Previously Presented): The computational unit of claim 7, wherein the pair of registers includes first and second registers and wherein the predetermined states include one or more of the following for the first and second registers, respectively: load, hold; load, clear; hold, load; clear, load; hold, hold; hold, clear; clear, hold; and clear, clear.

Claim 12 (Currently Amended): The computational unit of claim 7, wherein the control signal value comprises 7 bits to control loading the pairs of pipeline registers as accumulator pair enabling 72 bit operations in the computation unit.

Claim 13 (Previously Presented): An apparatus for providing a data value in a computational unit in an adaptable computing engine, wherein the computational unit includes a multi-stage execution pipeline, the apparatus comprising

one or more functional units coupled by a bus, wherein the one or more functional units include functional unit inputs;

at least one input register coupled between the bus and at least one functional unit input, the at least one register configured to store a value received from the bus at a beginning or end of a first clock cycle; and

a data path from the at least one input register to a given stage in the execution pipeline so that the value provided by the register is available for use at a time of execution of the given stage of the at least one functional unit, wherein the value is available to the given state at a next clock cycle from the first clock cycle.

Claim 14 (Previously Presented): The apparatus of claim 13, wherein the register includes circuitry for selectively providing a constant value.

Claim 15 (Previously Presented): A method for providing a data value in a computational unit in an adaptable computing engine, wherein the computational unit includes a multi-stage pipeline, the method comprising

coupling one or more functional units to a bus, wherein the one or more functional units include functional unit inputs;

coupling at least one register between the bus and at least one functional unit input;

storing a value received from the bus in the at least one register at a beginning or end of a first clock cycle: and

providing a data path from the at least one register to a given stage in the execution pipeline so that the value provided by the at least one register is available for use at a time of execution of the given stage of the at least one functional unit. wherein the value is available to the given state at a next clock cycle from the first clock cycle.

Claim 16 (Previously Presented): The apparatus of claim 13, wherein the register includes circuitry for selectively providing a constant value.

Claim 17 (Previously Presented): The method of claim 1, wherein the data value is obtained from the at least one register without performing an access command to memory.

Claim 18 (Previously Presented): The method of claim 7, wherein the data value is obtained from the at least one register without performing an access command to memory.

Claim 19 (Previously Presented): The apparatus of claim 13, wherein the data value is obtained from the at least one register without performing an access command to memory.

Claim 20 (Previously Presented): The method of claim 15, wherein the data value is obtained from the at least one register without performing an access command to memory.

Claim 22 (New): The method of claim 1 wherein a selected bit of the control signal determines whether one or both of the pipeline registers are loaded.